Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) In a controller of a computing device, the computing device comprising a system memory and a codec, a method being implemented by the controller comprising:

receiving a buffer descriptor list from a buffer descriptor list controller, the buffer descriptor list defining a plurality of buffer segments of a buffer to be read,

reading data from the buffer of the system memory via a first interface of the controller based, at least in part, on the buffer descriptor list,

transferring the data to the codec via a second interface of the controller,

tracking a position in the buffer from which the controller has read the data, and

writing a value to a direct memory access position-in-buffer (DPIB) structure located in the system memory via the first interface to indicate the position in the buffer, wherein the first interface is an isochronous interface that supports relaxed ordering rules.

2. (Previously Presented) The method of claim 1 wherein the reading comprises isochronously receiving the data via the first interface.

3. (Original) The method of claim 1 further comprising tracking progress of transferring the data to the codec via the second interface.

4. (Original) The method of claim 1 wherein reading the data from the buffer comprises reading the data per a buffer descriptor list that defines the buffer.

5. (Previously Presented) The method of claim 4, wherein reading the data from the buffer further comprises returning to a start of the buffer in response to reaching an end of the buffer.

6. (Previously Presented) The method of claim 1 further comprises, prior to writing the value to system memory, determining whether to update the value in the system memory based upon the data transferred via the second interface.

Claims 7-18 (Cancelled)

19. (Currently Amended) A controller comprising

a buffer descriptor list controller to provide a buffer descriptor list to a first direct memory access controller,

the ~~a~~ first direct memory access controller to transfer data between a system memory and a codec via a first interface to the system memory and a second interface to the codec based, at least in part, on the buffer descriptor list, and

a position controller to update a position value in a direct memory access position-in-buffer (DPIB) structure located in the system memory via the first interface to indicate progress of the first direct memory access controller in transferring data between the system memory and the codec, wherein the first interface is an isochronous interface that supports relaxed ordering rules.

20. (Original) The controller of claim 19 further comprising a second direct memory access controller

to read from the system memory a buffer descriptor list that defines a buffer in the system memory, and

to configure the first direct memory access controller to transfer the data between the buffer and the codec per the buffer descriptor list.

21. (Original) The controller of claim 19 further comprising a link counter to maintain a count indicating progress of the first direct memory access controller in transferring the data across the second interface.

22. (Original) The controller of claim 19 further comprising a buffer position counter to maintain a count indicating progress of the first direct memory access controller in transferring the data across the first interface.

23. (Original) The controller of claim 19 wherein the first direct memory access controller isochronously writes the data to the buffer.

24. (Original) The controller of claim 19 wherein the first direct memory access controller isochronously reads the data from the buffer.

Claims 25-28 (Cancelled)